

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listings of Claims:

1 1. (original) A nonvolatile memory comprising:
2 a memory array unit having a plurality of
3 nonvolatile memory cells; a control unit; and a voltage
4 generating unit for supplying voltages to said
5 nonvolatile memory cells,
6 wherein said nonvolatile memory cells store
7 information corresponding to the quantity of electric
8 charges in a floating gate of each nonvolatile memory cell,
9 wherein said control unit controls a write operation
10 to store information into said nonvolatile memory cells; a
11 read operation to read information stored in said
12 nonvolatile memory cells; and an erase operation to erase
13 information stored in said nonvolatile memory cells,
14 wherein said voltage generating unit has an erase
15 voltage generating unit for generating, in accordance with
16 control from said control unit, erase voltages to be
17 applied to said nonvolatile memory cells in said erase
18 operation, and

19 wh rein said erase voltage gen rating unit generates,
20 on the basis of a control signal supplied from said control
21 unit, erase voltages of two or more levels and applying
22 them to a control gate of each of said nonvolatile memory
23 cells.

1 2. (original) A nonvolatile memory comprising:
2 a memory array unit having a plurality of nonvolatile
3 memory cells; a control unit; and a voltage generating unit
4 for supplying voltages to said nonvolatile memory cells,
5 wherein said nonvolatile memory cells store
6 information corresponding to the quantity of electric
7 charges in a floating gate of each nonvolatile memory cell,
8 wherein said control unit controls a write operation
9 to store information into said nonvolatile memory cells; a
10 read operation to read information stored in said
11 nonvolatile memory cells; and an erase operation to erase
12 information stored in said nonvolatile memory cells,
13 wherein said voltage generating unit has an erase
14 voltage generating unit for generating, in accordance with
15 control from said control unit, erase voltages to be
16 applied to said nonvolatile memory cells in said erase
17 operation, and

18 wher in said erase voltage generating unit generat s,
19 on the basis of a control signal supplied from said control
20 unit, erase voltages of two or more levels to make the
21 voltages applied to the tunnel films of said nonvolatile
22 memory cells substantially constant and applies them to a
23 control gate of each of said nonvolatile memory cells.

1 3. (original) The nonvolatile memory according to
2 Claim 2, wherein said erase voltage generating unit, after
3 applying erase voltages of two or more different levels to
4 said control gates of said nonvolatile memory cells,
5 verifies the erase.

1 4. (original) The nonvolatile memory according to
2 Claim 3, wherein, out of the erase voltages generated by
3 said erase voltage generating unit, a first voltage level
4 of an erase voltage first applied to said control gate of
5 any of said nonvolatile memory cell is the lowest, and each
6 of the erase voltages applied second and afterwards is
7 higher in level than the erase voltage applied immediately
8 before.

5. (canceled)

6. (canceled)

7. (canceled)

1 8. (original) A nonvolatile memory comprising, on one
2 semiconductor substrate, a memory array unit; a control
3 unit; and a voltage generating unit,
4 wherein said memory array unit has a plurality of word
5 lines and a plurality of nonvolatile memory cells,
6 wherein each of the nonvolatile memory cells has a
7 first terminal connected to a first semiconductor region; a
8 second terminal connected to a second semiconductor region;
9 and a third terminal connected to a control gate;
10 wherein there is an electric charge accumulating
11 region above a channel region between said first
12 semiconductor region and said second semiconductor region
13 and between it and said control gate; and there is a first
14 insulating film between the electric charge accumulating
15 region and the channel region,
16 wherein the third terminal of at least one nonvolatile
17 memory cell is connected to each word line,
18 wherein data are stored into each nonvolatile memory
19 cell according to the quantity of electric charges

20 accumulat d in said electric charge accumulating region;
21 and the quantity of electric charges is controlled by the
22 control of said control unit over a first operation to
23 inject electric charges into said electric charge
24 accumulating region and a second operation to eject
25 electric charges out of said electric charge accumulating
26 region,

27 wherein, in order to perform said second operation, a
28 voltage generated by said voltage generating unit is
29 applied between said control gate and channel region via a
30 word line connected to the control gate, and

31 wherein, during the period of said second operation,
32 the voltage generated by said voltage generating unit is
33 varied twice or more, so as to keep the voltage applied to
34 said first insulating film within a predetermined voltage
35 range.

1 9. (original) The nonvolatile memory according to
2 Claim 8,

3 wherein, during said first operation, the voltage
4 generated by said voltage generating unit is applied
5 between said control gate and channel region via a word
6 line connect d to the control gate, and

7 wherein, during said first operation, the voltage
8 generated by said voltage generating unit is varied.

1 10. (original) The nonvolatile memory according to
2 Claim 9,

3 wherein, the voltage applied between said control gate
4 and channel region in said first operation differs in
5 polarity from the voltage applied between said control gate
6 and channel region in said second operation.

1 11. (original) The nonvolatile memory according to
2 Claim 10,

3 wherein the threshold voltage of the nonvolatile
4 memory cells is varied according to the quantity of
5 electric charges accumulated in said electric charge
6 accumulating region so as to be included in a plurality of
7 threshold voltage distributions according to data to be
8 stored into said nonvolatile memory cells,

9 wherein in said first operation, the threshold voltage
10 of the nonvolatile memory cells are moved into a first
11 threshold voltage distribution, and a first determination
12 is made during said first operation as to whether or not

13 the threshold voltage of the nonvolatile memory cells are
14 moved within said first threshold voltage distribution,
15 wherein in said second operation, the threshold
16 voltage of the nonvolatile memory cells are moved into a
17 second threshold voltage distribution; and a second
18 determination is made during said second operation as to
19 whether or not the threshold voltage of the nonvolatile
20 memory cells are moved within said second threshold voltage
21 distribution,
22 wherein said threshold voltage of at least one of a
23 plurality of nonvolatile memory cells connected to one
24 word line is moved, in said first operation, and
25 wherein said threshold voltages of all of the plural
26 nonvolatile memory cells connected to one word line are
27 moved, in said second operation.